Review8. The Processor

2019年6月2日

10:07

Hint: Bold - formula, underline - important, italic - not so important, grey - not so sure.

Implementation overview

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image001.png
  + Instruction count: ISA (Instruction set architecture) and compiler.
  + CPI and cycle time: CPU hardware.
* Basic MIPS architecture: math, memory access, branch and jump.
  + Implementation: memory, registers, ALU, and control logics, CPU operations.
* Overall implementation design:

PC 
4 
Address Instruction 
Instruction 
Ad 
Register 
Registers 
Register # 
Reg Ster # 
ALU 
Address 
Data 
memory 

* Two add units: first add unit increases PC value by 4; second add unit compute J-type instructions' address (offset \* 4 + PC).
* Into data memory: memory instructions address after shamt, or arithmetic result.
* Into ALU: registers $rs, $rt from R-type instruction or immediate value from I-type instruction; data from arithmetic computation.
* Into register unit: new data or address from ALU.

Logic design basics

* Combinational elements: operate on data and output is a function of inputs.
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image003.png
* Sequential elements (state elements): store information.
  + Sequential without write control: PC, determined by posedge of clk.
  + Sequential with write control: data memory / register, updates on posedge of clk when write control is 1.
    - Data memory: <input> 32 bit address, 32 bit write data, 1 bit MemWrite, 1 bit MemRead; <output> 32 bit read data. - Read and Write.
    - Instruction memory: <input> 32 bit instruction address, 1 bit clk; <output> instruction. - Read only.
    - Registers: <input> 3 registers of 5 bit, 32 bit write data, 1 bit RegWrite; <output> 2 read data of 32 bit. - Read and Write.
* Units need clock: PC, instruction memory, registers, and data memory.
* Saved data in posedge of clk: PC (address of instruction), instruction, register, data, data memory address.

Detailed implementation for every instruction

* R-type instructions: read data from two registers, if RegWrite valid, then write data back to the third register.

4 
寄 存 器 号 
数 据 
5 
读 寄 存 器 1 
读 数 据 1 
5 
读 寄 存 器 2 
寄 存 器 
5 
写 寄 存 器 
读 数 据 2 
写 数 据 
RegWrite 
数 据 
ALUOp 
零 标 志 
ALU 
ALU 结 果 

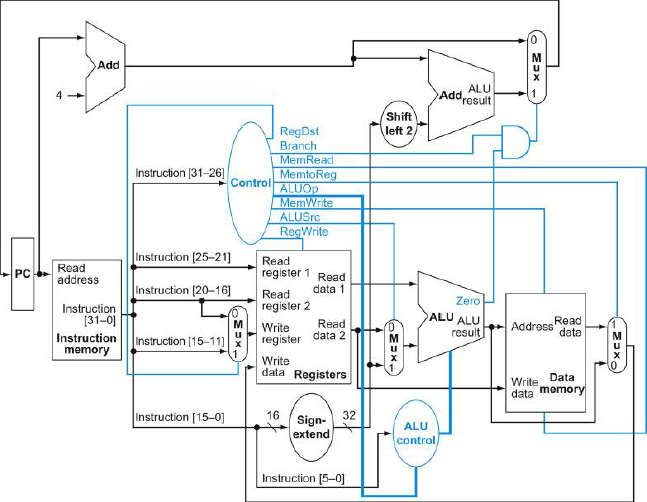
* *Input two register number of 5 bit and output 2 read data from registers of 32 bit, then input into ALU. Get result and back into write data. If RegWrite valid, write data into write register.*
* Loads / stores instructions: lw and sw, two read registers (two read data), one write register and one write data.

Register 
numbers 
a. Registers 
5 
5 
5 
Read 
register 1 
Read 
register 2 
Registers 
Write 
register 
Write 
Data 
Read 
data 1 
data 2 
RegWrite 
ALU operation 
4 
Zero 
ALU ALU 
result 
MernWr ite 
Address 
Where does this input come from? 
Write 
data 
data 
memory 
MemRead 

* Right bottom is data memory, two controls are MemWrite and MemRead. ALU result goes into address, and read data 2 goes into write data.
* Input of ALU comes from two read data.
* J-type instructions: offset should be left shift 2 bits, so can be store 4 times more offset address. Therefore, before use, offset should be left shift 2 bits.

PC 4 from 
data 1 
register 2 
Wrie Registers 
Shin 

* Overall control signals:



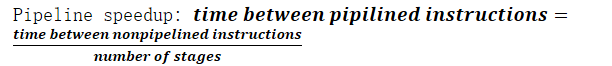
* RegDst: assign the write register, $rd (1) or $rt (0).
* Branch: whether an instruction is a branch instruction.
* MemRead: control data memory to read data from address (lw).
* MemtoReg: choose source to write into register, memory-read-data (1) or ALU result (0).
* ALUOp: from function code to determine operation ALU should operate.
* MemWrite: control data memory to write data to address (sw).
* ALUSrc: determine the input of ALU, sign extend immediate value (1) or $rt (0).
* RegWrite: enable to write to registers.

Review9. The Overview of Pipeline

2019年6月2日

10:07

Pipeline design and performance

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image008.png
* Stages of pipeline: IF (instruction fetch), ID (instruction decode & register read), EX (execute ALU), MEM (memory access), WB (write back).
  + *Left Reg means write, and right Reg means read.*
* 
  + Latency: time for each instruction.

Hazards

* Structure hazards: required resource is busy.
  + *Hardware problem, use separate memories of instruction and data.*
* Data hazards: wait for data read / write.
  + Forwarding: use result from ALU immediately into register read.
  + Load-use data hazard: use data from lw, solved by reorder.
* Control hazards: decisions depends on previous instruction.
  + Branch prediction: static (typical branch behavior) and dynamic (hardware record recent branch).

Review10. Instruction-Level Parallelism

2019年6月2日

10:07

Multiple issue

* Instruction level parallelism (LIP): deeper pipeline, or multiple issue.
* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image010.png
* Static multiple issue by compiler and dynamic multiple issue by processor.
  + Static multiple issue: instructions into issue packets (very long instruction word, VLIW).
    - *Hazards: data hazard split into two packets.*
* Dynamic multiple issue (superscalar processor): CPU makes decision and no need for compiler scheduling.
* Speculation: guess and start operation as soon as possible.
  + Compiler reorder and hardware looks ahead for instructions (buffer results and flush on incorrect speculation).
  + Exceptions: static speculation add ISA support for deferring exceptions, dynamic speculation buffers exceptions until instruction completion.

Multiple issue scheduling

* Static multiple issue scheduling: reorder, dependencies between packets, pad with nop.
* An ALU / branch, load / store two packages multiple issue example:

Loop: 
Loop: 
addu 
sw 
addi 
bne 
$tO, 
$tO, 
SSI, 
$sl, 
O($sl) 
O($sl) 
SSI, —4 
$zero, 
$tO=array el ement 
add scalar in Ss2 
store result 
decrement poi nter 
branch 
ALIJ/branch 
LOOP # 
Load/store 
nop 
addi 
addu 
bne 
IPC 
SSI, SSI, —4 
sto, sto, ss2 
SSI, 
Sze ro, Loop 
lw sto, OCSSI) 
nop 
nop 
sw sto, 4(ss1) 
cycle 
1 
2 
3 
4 
= 5/4 = 1.25 (c.f. peak IPC = 2) 

* *Replicate loop body: expand loop several times and use different registers (register renaming).*
  + *Anti-dependencies (name dependence): no data flow between two instructions, only because of the name of register.*

IPC = 14/8 = 1.75 
• Closer to 2, but at cost of registers and code size 
SSI, -16 
sto, sto, 
stl, stl, 
St2, St2, 
St3, st3, 
AL IJ/branch 
Loop : 
addi 
nop 
addu 
addu 
addu 
addu 
nop 
bne 
SSI, 
ss2 
SS2 
ss2 
SSI, Szero, Loop 
Load/store 
sto, 
sti, 
st2, 
st3, 
Sto, 
sti, 
st2, 
st3, 
O(SSI) 
12 (SSI) 
scssl) 
4(SS1) 
16(SS1) 
12 (SSI) 
8(SS1) 
4(SS1) 
cycle 
1 
2 
3 
4 
6 
7 
8 

* Hardware support, CPU executes out of order (commit result to registers in order).

Instruction tetch 
and decode unit 
Reservation 
station 
Functional 
Intew 
units 
Reorders buffer for 
Reservation 
station 
Integer 
Commit 
Reservation 
station 
Floating 
point 
In-order issue 
Reservation 
station 
Out-of-order execute 
In-order commit 
an supp y 
issued 
Id pending 
ts also sent to 
y waiting 

* One IF / ID unit, several functional units, and one commit unit.

Review11. Large and Fast: Exploiting Memory Hierarchy

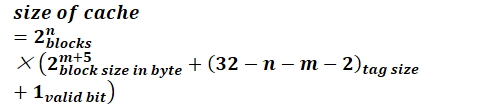
2019年6月2日

10:07

Memory

* DRAM (high bit density but poor latency) store data and instructions, SRAM designs cache.
  + Registers > L1 cache > L2 cache > memory > disk.
  + Memory in unit of byte or in unit of word.
* Cache: block is unit of copying.
  + *Miss, miss penalty, and miss ratio - hit.*
  + Temporal locality and spatial locality.
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image014.png
* DRAM: refresh to keep data. Store in bank, with several row, and each row has several column.
  + *Pre to open / close a bank and act to access one or several (burst mode) rows (into buffer).*
  + *SDRAM (synchronous DRAM) adds a clock to synchronize with processor. Burst mode won't send multiple addresses.*
    - *DDR (double data rate) DRAM: transfer on both sides of clock.*
* Flash: nonvolatile semiconductor storage.
  + *Flash bits wears out, and use wear leveling to remap data to less used blocks.*
* Disk: nonvolatile rotating magnetic storage.
  + *Track, sector, queuing delay, seek (find track), rotational latency, data transfer, controller overhead.*

Cache map

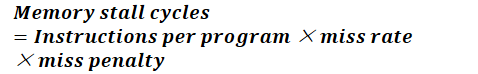
* Direct mapped cache: index, valid bit, tag, and data.
  + Index: from 0 to n - 1 of cache size, which is lower bits of memory address.
  + Tag: high order bits of memory address.
  + Valid bit: whether there is data in a location.
  + Data: data from memory.
* For unit of word memory, two bits of byte offset determines which byte to access.
* Larger block size: can be considered as more offset bits.
  + For 32 bits address, block size m word (m+2 bits), n bits of index:
    - C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image015.png
    - C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image016.png
    - 
* Cache miss: stall CPU pipeline and fetch block (instruction cache miss and data cache miss).
* Write through (update memory on cache change, use write buffer) and write back (update memory when leave cache, and log dirty bit).
* *Write allocate: on write miss,*
  + *Write through (alternatives): allocate and fetch the block, or write around and don't fetch the block.*
  + *Write back: fetch the block, in fact much complex.*

Review12. Memory Performance and Dependable Memory Hierarchy

2019年6月2日

10:07

Cache performance

* CPU time: program execution cycles and memory stall cycles.
  + 
  + I-cache (instruction cache) miss and D-cache (data cache) miss: all instructions can cause I-cache miss, while only lw / sw can cause D-cache miss.
* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image019.png

Associative caches

* Group blocks into set: n-way associative n blocks in one set, fully associative n blocks in one set.

31 30... 12 1098...3210 
Inftx 
v 
Ta 
Data 
Data 
O ata 
4-to-l multiplex 

* N-way associative needs n comparator, and search n times, and n places to put blocks.
* Replacement policy: non-valid, then LRU (least-recently used), or random (approximately LRU for high associativity).

Multilevel caches

* Primary cache minimal hit time, L-2 cache low miss rate.
* *Service accomplishment failure to service interruption, then restore.*
  + *Reliability: MTTF (mean time to failure).*
  + *Service interruption: MTTR (mean time to repair).*
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image021.png
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image022.png

The Hamming SEC code

* Hamming distance: number of different bits between two bit pattern.
  + Distance 2 (parity code) SED, distance 3 SEC / DED.
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image023.png
* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image024.png

Encxdeddatebts 
PI dl d2 d3 d4 

* Encode and decode, error of parity bits can identify error position.
* SEC / DED code: add an additional parity bit for whole word pn.
  + Hamming distance becomes 4.
  + H is SEC parity bits: H zero pn even no error, pn odd pn error. H non-zero pn odd correct one error, pn even detect double error.
    - The additional bit is at the end of pattern. H is the calculated SEC parity bits after transfer (without consider additional bit).
    - Recalculate H and pn, according to even-odd decides error (in fact, consider H whether 0 in actual use).
  + Can detect at most 3 error, but don't know exactly which bit wrong, and would mix with SEC, then leads to wrong correction.

Review13. Virtual Memory

2019年6月2日

10:07

Virtual memory

* Programs share main memory and use private virtual memory.
  + VM page - block, VM page fault - miss.
* Page table: index PTE (page table entries) by virtual page number.

Page table register 
Virtual 
31 30 29 2B 27.... ..15 14 13 12 
V i rtual 
Physical page number 
O is not 
present in 
11109 e 
• •-321 
Page offset 
29 28 '4 '3 '2 10 9 e, 
210 
Physical page r 
Physical address 
Page Offset 

* Page table register in CPU and page table in memory.
* PTE: stores physical page number, referenced, dirty, valid…
* Page not present: PTE refer to location in swap space on disk.
* Replacement: LRU replacement using reference bit (use bit).
* Write: use write-back and set dirty bit in PTE.

Fast translation using TLB

* TLB (translation lookaside buffer): store recently used PTEs.

a6e101S 
001 
ssaappp ΙΟ 
a6ed 
Olqel a6ed 
6e1 
36ed lea!sA14d 
00 0 
»aqumu 
a6ed 

* Tag stores high bits of PTE virtual memory address.
* TLB miss: search PTE in memory.
  + Page in memory: load PTE and retry.
    - *Hardware design more complicated page table, software raises a special exception.*
  + Page not in memory: page fault, *OS handles fetching page and restart the faulting instruction.*
* TLB to find address and cache to find data.

Memory hierarchy

* *Memory protection: tasks share parts of their virtual address spaces.*
  + *Privileged supervisor mode (kernel mode).*
  + *Privileged instructions and read only data (page table, state information).*
  + *Switch between kernel mode and user mode (system call exception).*
* *Block placement: direct map, n-way set associative, and fully associative.*
* Finding a block: full lookup table of fully associative cost 0 comparison.
* *Replacement on a miss: LRU or random.*
  + Virtual memory uses LRU approximation with hardware support while cache uses either LRU or random.
* *Write policy: write-through with write buffer, write-back with more states.*
* Sources of misses: compulsory miss (cold start miss), capacity miss, conflict miss (collision miss).

Design change 
Increase cache size 
Increase associativity 
Increase block size 
Effect on miss rate 
Decrease capacity 
mlsses 
Decrease conflict misses 
Decrease compulsory 
misses 
Negative performance 
effect 
May increase access 
time 
May increase access 
time 
Increases miss penalty. 
For very large block size, 
may increase miss rate 
due to pollution. 

Virtual machines

* *Host computer emulates guest operating system and machine resources.*
  + *Improve isolation, avoid security and reliability problems, share resources.*
  + *Has some performance impact.*
* *Virtual machine monitor:*
  + *Maps virtual resources to physical resources.*
  + *Guest in user mode while VMM in privileged supervisor mode.*
  + *Guest OS different from host OS.*
  + *VMM handles real I/O devices and emulates for guest.*
* *Instruction set support.*

Review14. Parallel Processors from Client to Cloud

2019年6月2日

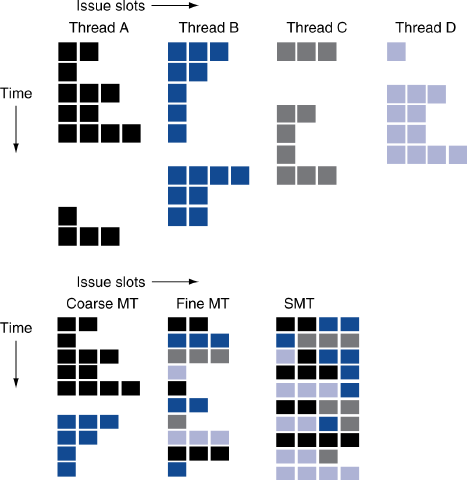
10:07

Multiprocessors

* *Parallel processing program: efficiently executed.*
  + Hardware: serial and parallel.
  + Software: sequential and concurrent.
* Parallel and scaling: partition, coordination, and communication overhead.
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image029.png
  + Strong scaling: problem size fixed.
  + Weak scaling: problem size increases due to number of processors increases.
* *Load balancing: each processor has same number of tasks.*

Level parallelism

* Parallel processing: SISD (single instruction stream, single data stream), MIMD (multiple instruction multiple data), SPMD (single program multiple data), SIMD (single instruction multiple data), and vector.
  + SPMD: program on a multi-core processor, different processor execute on different sections of code.
  + SIMD: operate on vectors of data (data level parallelism), processors execute same instruction on different data address.
  + Vector processors: designed for vector operation, pipelined execution units.
* Multithreading: related to MIMD, multiple threads share a single processor.
  + *Fine-grain multithreading: switch threads, interleave instruction execution, and execute other threads when one is stall.*
  + SMT (simultaneous multithreading): multiple-issue dynamically scheduled processor.



Multicore microprocessors

* *SMP (shared memory multiprocessor): efficiently programming on multiprocessor.*

Processor 
processo r 
Cache 
Interconnection Network 

* Message parsing multiprocessors: each processor has private physical address space, and share messages via hardware.

Р Сосе 550' 
саспе 
Метогу 
Processor 
саспе 
Мет 0 '-у 
Interconnection Netw0rk 
сасће 

* *Loosely coupled clusters: network of independent computers.*
* *Cloud computer: WSC (warehouse scale computers), SaaS (software as a service), PMD (personal mobile device) or cloud running software.*
* *Data center: computers connected by off-the-shelf networking devices.*

Other processor units

* *GPU (graphic processing unit): highly data-parallel processing, oriented towards bandwidth.*
* *TPU (tensor processing unit): tensorflow platform.*
* *DPU (deep learning processing unit): FPGA-based processing unit.*
* *NPU (neural network processing unit): IBM TrueNorth.*
* *BPU (brain processing unit).*

Review15. Final Review

2019年6月2日

10:07

The processor

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image001.png
* Units of CPU: PC, memory (instruction, data), registers, ALU.
  + MUX ternary operator, and ALU function.
  + R-type, lw / sw, J-type instructions.
* Control signals: RegDst, Branch, MemRead, ALUOp, MemWrite, ALUSrc, RegWrite.

The overview of pipeline

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image033.png
* Stages of pipeline: IF, ID, EXE, MEM, WB.
* Hazards: structure, data (forwarding, load-use), control.

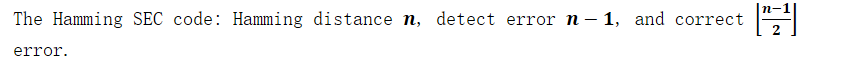
Instruction-level parallelism

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image034.png
* Multiple issue: static (compiler), dynamic (hardware).
  + Speculation with reorder and buffer.
  + Exception handler.
* Multiple issue scheduling: replicate loop body.

Large and fast: exploiting memory hierarchy

* Memory: SRAM, DRAM, flash, disk.
* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image035.png
* Cache map: index, valid bit, tag, data.
  + Write-through (buffer, allocation), write-back (complex, read textbook).

Memory performance and dependable memory hierarchy

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image036.png
* Instruction cache miss and data cache miss.
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image037.png
* Associative cache: direct map, n-way associative, fully associative.
  + Replacement: non-valid, LRU, random.
* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image038.png
  + C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image039.png
* 
  + Parity bits and data bits, additional parity bit (SEC / DED).

Virtual memory

* VM page, VM page fault.
* Page table (memory): valid bit, dirty bit, reference bit, physical address.
* TLB (cache): valid bit, dirty bit, reference bit, tag, physical address.
* Memory hierarchy: direct map, n-way associative, fully associative (search n entries, full lookup table), .
  + Replacement: LRU approximate with hardware support.
  + Miss: compulsory miss, capacity miss, conflict miss.

Parallel processors from client to cloud

* C:\8C796445\C61A9132-5FE2-4411-A7E8-2653F5DDF17A.files\image041.png
* Strong scaling and weak scaling, load balancing.
* Parallel processing (single core): SISD, MIMD, SPMD, SIMD, vector processor, multithreading (SMT).
  + Multicore: SMP, message parsing multiprocessor, cluster, cloud, data center.